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Design and Implementation of an Efficient 64 bit MAC

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ABSTRACT
The design of optimized 64 bit multiplier and accumulator (MAC) unit is implemented in this paper. MAC unit plays major role in many of the digital signal processing (DSP) applications. The MAC unit is designed with the combinations of multipliers and adders. In the proposed method MAC unit is implemented using Vedic multiplier and the adder is done with ripple carry adder .The components are reduced by implementing Vedic multiplier using the techniques of Vedic mathematics that have been modified to improve performance. a high speed processor depends significantly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. The area is optimized effectively using Vedic multiplier .The total design implemented using Xilinx.
Keywords-Carry save adder, Digital signal processing (DSP), multiplier and accumulator (MAC)

I. INTRODUCTION

We have entered in the digital domain where the digital signal processing is of main concern. The performance of DSP is mainly dependent upon the MAC unit. So by optimizing the MAC unit we can optimize performance of the Digital Signal Processors, and in MAC unit Multiplication is the main operation where our proposed design of MAC unit can be very useful. Multiplication is the most time consuming amongst the basic mathematical calculation. With these considerations, it is always important to have fast and efficient mechanism to implement mathematical functions.

Vedic Mathematics is a name which is heard many times with reference to the techniques for solving mathematics problem mentally. One of the main purposes of Vedic mathematics is to transform the tedious calculations into simpler, orally manageable operation without much help of pen and paper. Any ordinary human can perform mental operations for very small magnitude of numbers and hence Vedic mathematics provides techniques to solve operations with large magnitude of numbers easily. Vedic mathematics provides more than one method for multiplication operations. For each operation there is at least one generic method provided along with some methods which are directed towards specific cases simplifying the calculations further. Vedic mathematics provides algorithms to simplify the mathematics and hence is perfect solution for the problem stated. After a thorough and comparative study we have found that Vedic multiplier designed by is better than other available multipliers. A MAC unit consists of a multiplier, adder and an accumulator containing the sum of the previous successive products. The MAC Unit obtain inputs from the memory location such as RAM and given to the Multiplier.MAC Unit is used in DSP Applications that uses discrete cosine transform (DCT) or discrete wavelet transforms (DWT). Where, Multiplication is accomplished by repetitive application of addition, the speed of the multiplication and addition arithmetic determines the execution speed and performance of the entire Calculation. The functionality of the MAC unit enables high-speed filtering and other processing which are typical for DSP applications.

Particularly, in applications like optical Communication Systems which is based on DSP, require extremely fast processing of huge amount of digital data.

II. MAC UNIT

The Multiplier-Accumulator (MAC) operation is the key operation not only in DSP applications but also in multimedia information processing and various other applications. As mentioned above, MAC unit consist of multiplier, adder and register/accumulator. In this paper, we used 64 bit modified Wallace multiplier. The MAC Unit take inputs from the memory location such as RAM and given to the multiplier block. This is very useful in 64 bit digital signal processor. The input which is being fed from the memory location is 64 bit. When the input is given to the multiplier it starts computing value for the given 64 bit input and hence the output will be 128 bits. The multiplier output is given as the input to carry save adder (CSA) which performs addition. The function of the MAC unit is given by the following equation

$$Y = \sum_{i=0}^{63} A_i \times B_i \qquad \text{--------(1)}$$

Where, Ai & Bi are two 64 bit input Operands, Y is the output of MAC Unit and i is a 64 bit value. This Equation performs Summation of partial products. The Carry Save Adder (CSA) produces 129 bit output. Since, one bit is for the carry (128 bits + 1 bit). Then, the output of CSA is given to the accumulator register. The accumulator used is designed with Parallel in Parallel out (PIPO) type. Because the CSA Produces output in Parallel form and also the bits are huge. PIPO register is used where the input bits are given in parallel and output is taken in parallel.

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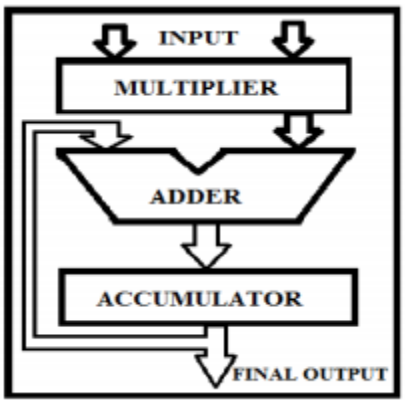

Fig.1 Architecture of MAC

The architecture of the designed MAC unit is shown in the figure 1. The two input 64 bit operand to the MAC unit are A [63:0] and B [63:0].The 64 bit output from MAC unit is Q [127:0]. The proposed design uses one 64x64 Vedic multiplier using Urdhva Tiryakbhyam algorithm. 128 bit accumulator using Ripple carry adder and one 128 bit register. Vedic multiplier design can increase MAC unit design speed and reduce the Area.

Thus 64 bit Modified Wallace Tree Multiplier is constructed and the total number of stages in the second phase is ten. As per the equation the number of row in each of the ten stages was calculated and the use of half adders was restricted only to the Tenth stage. The total number of half adders used in the second phase is eight and the total number of full adders that was used during the second phase is slightly increased that in the Conventional Wallace Tree Multiplier. Since, the 64 bit Modified Wallace Tree Multiplier Representation is very difficult, A Typical 10 bit by 10 bit in the Modified Wallace Tree shows better Performance when CSA is used in final stage instead of Ripple Carry Adder (RCA). The Carry Save Adder (CSA) is a type of Digital Adder, used to compute the sum of three or more number of bits in binary form. CSA gives less propagation delay and the glitching problem in RCA is also avoided. Since, the Representation of 128 bit CSA is very difficult.

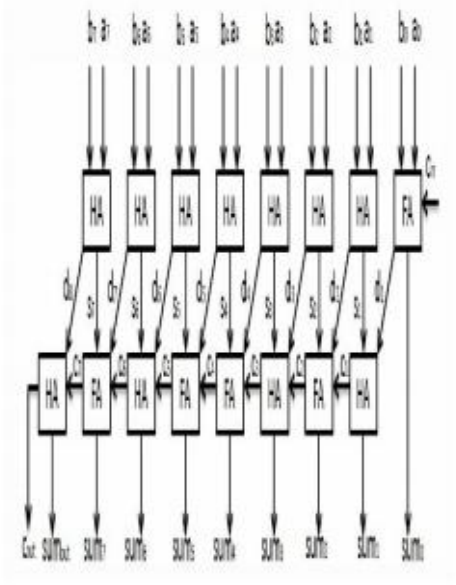

Fig.2 CARRY SAVE ADDER

Here, we compute the sum of two 128 bit binary numbers so 128 half adders at the first stage is required instead of 128 full adders. Since, we add bits of two binary numbers only. Each black cell consists of two AND gates and one OR gate. Multiplexer is combinational circuit which consists of multiple inputs and a single output. Each gray cell consists of only one AND gate. Pi denotes propagate and it consists of only one AND gate [5] given in equation 2. Gi denotes generate and it consists of one AND gate and OR gate [6] given in equation 3.

$$P_i = B_i \text{ AND } B_{i-1} \qquad \text{---------- (2)}$$

$$G_i = A_i \text{ OR } [B_i \text{ AND } A_{i-1}] \qquad \text{-- (3)}$$

III. RESULT

The design is developed using VHDL, and the previous work 64 bit MAC unit is designed using

Modified Wallace multiplier. The LUT's, Slices and IOB's comparative table are shown in the table1. Simulation Waveform of 64 bit MAC unit are shown in Fig. 3

Fig.3 Output Waveform

SYNTHESIS REPORT	WALLACE	VEDIC
NO.OF LUTS	239 OUT OF 10944 (2%)	129 OUT OF 10944 (1%)
NO OF SLICES	198 OUT OF5472 (3%)	79 OUT OF 5472 (1%)
TOTAL NO OF LUTS	268 OUT OF 10944 (2%)	158 OUT OF 10944 (1%)
NO OF IOB'S	268 OUT OF 320 (85%)	256 OUT OF 320 (80%)

Table. 1 LUT's, Slices and IOB's

IV. CONCLUSION

This paper presents a highly efficient optimized of MAC unit is implemented using Vedic multiplier and the adder is done with ripple carry adder. The components are reduced by implementing Vedic multiplier using the techniques of "urdhva tiryakbhyam sutra" based on Vedic mathematics is modified to improve performance. a high speed processor depends significantly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. The area is optimized effectively using Vedic multiplier .it is observed that the Vedic multiplier is much more efficient than Wallace multiplier in terms of area. An awareness of Vedic mathematics can be effectively improved if it is integrated in engineering education.

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